Zurich University of Applied Sciences

School of Engineering

t.SCD - System on Chip Design

Person responsible for the course:	Hans-Joachim Gelke, gelk
Responsible OU:	
ECTS:	4
Valid for:	2012/2013
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Expertise:

- Integrate ready designed Intellectual Property Blocks into a design
- Implementing a 32-bit Soft Core RISC Processor
- Configuring FPGA hard Core Blocks like Memories and PLLs
- Setting up a development environment for the Soft Core Processor
- Setting Timing Constraints and running Timing Analysis for IC Design
- Clocking Concept and Clock Distribution

Methodological skills:

- Developing a technical concept for a programmable Device
- Managing a complete FPGA design flow from VHDL Design until generating the Bit-Map
- Planning script based tests
- Trouble shooting a FPGA design

Social skills:

- Cooperating in a design team

Personal skills:

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Learning objectives:

After completing this course the Student is enabled to:

- Explain the differences between the programmable logic architectures of devices on the market.
- Developing a programmable logic device with softcore processor from concept to bit map
- Integrating and testing third party ip blocks into a design
- Setting up a development environment for Soft Core Processors
- Writing script based testbenches

-Designing a correct clock distribution

Course content:

- How to use a SoC tool to configure Intellectual Property (IP)
- Implementing a 32-bit RISC Soft Core Processor with cache
- Utilizing FPGA Hard IPs like RAMs, FIFOs and PLLs
- Advanced Testbench Design
- Timing Analysis and Synthesis optimization
- Implementing Digital System Processing using Mathworks Simulink
- ARM Cortex based Hard Processor Systems (HPS)

Previous knowledge:

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Teaching method:

Type of lesson:	Number of lessons per week:
Lecture	14 * 2
Tutorial/Practicum	7 * 4
Block instruction	

Assessment:

According to the table or as specified in writing by the lecture at the beginning of the semester!

description	type	form	scope	assessment	weighting
Performance records during school hours	Lab Exercises, Short Test	Oral, Multiple choice	45 min.	1-6	30%
Semester end exam	Test	written	90 min.	1-6	30%

Language of instruction:

English

Instruction material:

- Slides with comments
- Script (German)

Additional literature:

- Lehmann, Wunder, Selz: Introduction to VHDl Design

Comments:

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