t.SCD - System on Chip Design

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verantwortliche OE:	
ECTS:	4
Schuljahr:	2012/2013
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Fachkompetenz:

- Integrate ready designed Intellectual Property Blocks into a design

- Implementing a 32-bit Soft Core RISC Processor

- Configuring FPGA hard Core Blocks like Memories and PLLs

- Setting up a development environment for the Soft Core Processor

- Setting Timing Constraints and running Timing Analysis for IC Design

- Clocking Concept and Clock Distribution

Methodenkompetenz:

- Developing a technical concept for a programmable Device

- Managing a complete FPGA design flow from VHDL Design until generating the Bit-Map

- Planning script based tests

- Trouble shooting a FPGA design

Sozialkompetenz:

- Working in a design team

Selbstkompetenz:

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Lernziel:

After completing this course the Student is enabled to:

- Explain the differences between the programmable logic architectures of devices on the market.

- Developing a programmable logic device with softcore processor from concept to bit map

- Integrating and testing third party ip blocks into a design

- Setting up a development environment for Soft Core Processors

- Writing script based testbenches

-Designing a correct clock distribution

- Setting timing constraints and running a timing analysis

Lerninhalt:

- How to use a SoC tool to configure Intellectual Property (IP)

- Implementing a 32-bit RISC Soft Core Processor with cache

- Utilizing FPGA Hard IPs like RAMs, FIFOs and PLLs

- Advanced Testbench Design

- Timing Analysis and Synthesis optimization

- Implementing Digital System Processing using Mathworks Simulink

- ARM Cortex based Hard Processor Systems (HPS)

Vorkenntnisse:

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Durchführung:

Unterrichtsart	Anzahl Lektionen pro Woche
Vorlesung	14 * 2
Übung/Praktika	7 * 4
Blockunterricht	

Leistungsnachweise:

Laut Tabelle oder gemäss schriftlicher Festlegung des Dozierenden zu Semesterbeginn!

Bezeichnung	Art	Form	Umfang	Bewertung	Gewichtung
Leistungsnachweise während Unterrichtszeit	Shorttest, Labs	oral, multiple choice	45 min.	1-6	30%
Semesterendprüfung	Test	written	90 min.	1-6	70%

Unterrichtssprache:

Englisch

Unterrichtsunterlagen:

- Slides with Comments

- Script (German)

Ergänzende Literatur:

- Lehmann, Wunder, Selz: Introduction to VHDl Design

Bemerkungen:

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